

EVRDA012M4

12 Bit 1.2 GS/s 4:1 MUXDAC Evaluation Board

Features

- ◆ Option of 2 mating connector board for input: UHD or SMA
- ◆ On-Board Balun Conveniently Converts High-Speed Clock Input to Differential Clock
- ◆ Evaluate in 4:1 and 2:1 mode
- ◆ Fully Assembled and Tested MUXDAC for your evaluation and prototyping needs

Product Description

The EVRDA012M4 is an evaluation board designed to demonstrate the performance of the RDA012M4 (MUXDAC), a 1.2GS/s, multiplexing digital-to-analog converter IC. The multiplexed input feature eases the requirement for the data interface. The evaluation kit consists of two assembled printed circuit boards: one hosting the MUXDAC IC, and one the input connection.

There are two different input boards available, allowing the user to select SMA or UHD connectors.

A third option is to use the Teledyne Scientifics' programmable data generator (RGA012M4) to supply the data. The data generator board allows the user to evaluate the MUXDAC without any data generating equipment. Only a sampling clock input is required.

For added convenience, the input high speed clock is converted on board into a differential clock using a high-frequency balun.

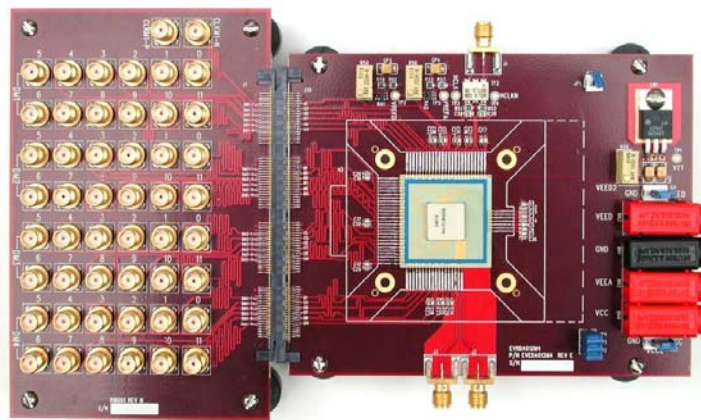


Figure 1 – EVRDA012M4-HD-SMA

Ordering information

| PART NUMBER | DESCRIPTION |
|-------------------|--|
| EVRDA012M4-HD-SMA | RDA012M4-HD Evaluation Board w/ SMA Input Connection Board |
| EVRDA012M4-HD-UHD | RDA012M4-HD Evaluation Board w/ UHD Input Connection Board |

Signal Description

Power Supplies

The evaluation board requires both a negative and positive supply voltage, and separate digital and analog supplies. VEEA is the analog $-5.2V$ supply, VEED is the digital $-5.2V$ supply. VCC is a $+3.3V$ supply needed for the digital interface. JU1 and JU2 are used to power down the unused logic when in 2:1 mode.

Connect the power supplies to the evaluation board using banana cables. There is no need for power-up sequencing.

Inputs

The EVRDA012M4 has three mating options for input. For connector based data input, the user may choose the SMA connector mating board, or UHD (Ultra High Density from Gore) mating board. The third option is the Teledyne Scientifics' RGA012M4, a programmable FPGA-based data generator board. This board allows users to program their own data vectors for the MUXDAC to sample. All that must be provided is the external sampling clock for the EVRDA012M4. See the RGA012M4 user guide for more information.

The EVRDA012M4 data input is NMOS ($3.3V$) compatible with Bit(11) being the input most significant bit (MSB) and Bit(0) the least significant bit (LSB).

The termination on data input lines are grounded through JP2, JP3, and JP4. By not having the termination directly connected to ground allows the

use of different data input standards, like HSTL-I which have a termination voltage of $0.75V$.

The default mode of the MUXDAC is 4:1 multiplexing mode. The jumper JP1 controls the SEL (mode SElection) signal, which selects the multiplexing operating mode. Leave JP1 uncapped for 4:1 mode or jump it for a 2:1 multiplexing mode.

The input clock signal is supplied through an SMA connector, J1, and is converted into a differential signal through a high frequency balun. The differential clock can be checked at TP3 and TP4.

VREFA and VREFD are $-2V$ references that are derived from the power supplies and made available to the MUXDAC. Potentiometer R56 and R50 in this circuit may have to be adjusted to achieve the nominal $-2V$. Test points are provided for probing purposes. It is a good idea to check that VREFA and VREFD are nominally $-2V$ after power up to achieve optimum performance from the MUXDAC. Likewise, potentiometer R58 may need adjustment to ensure a VTT value of $-1.3V$, the termination voltage for the differential sampling clock.

Outputs

The analog output (OUTP, OUTN) of the MUXDAC is available on the SMA connectors J2 and J3. OUTP and OUTN should be terminated with 50Ω impedance to ground.

The data clock (LCLKP, LCLKN) is LVDS compatible and its frequency is determined by the multiplexing mode, HCLK divided by 4 for 4:1 mode and HCLK divided by 2 for 2:1 mode. It should be terminated with differential 100Ω impedance at the receiving side.

PC Board Layout

The EVRDA012M4 is fabricated using six layers of FR4 material. Interface to the input board is through the QSE-080-01-F-D-EM2 high-speed edge connector from Samtec.

All data and clock signals are treated as 50Ω transmission lines. Figure 2 is the layer stack of the evaluation board, including layer thickness.

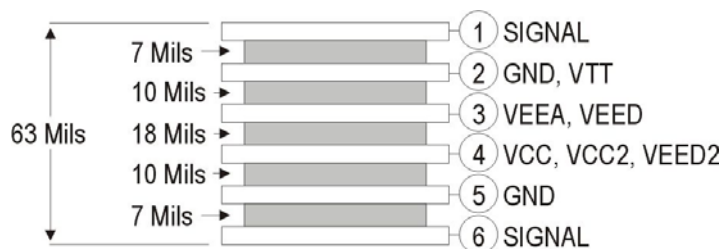


Figure 2 - EVRDA012M4 layer stack

Components

Table 1: Jumper and Test Point List

| DESIGNATOR / SIGNAL | SETTINGS | FUNCTION |
|-----------------------------|---|---|
| JP1 / SEL (Mux-Mode-Select) | OFF: SEL is HIGH ON: Link SEL to GND | OFF: 4:1 multiplexing mode ON: 2:1 multiplexing mode |
| JP2, JP3, JP4 / DTERM | ON: connect data termination to ground | Set data termination voltage |
| TP1 / VTT | Nominally -1.3V | Test point |
| TP2 / VREFD | Between -1.8V and -2.2V | Test point |
| TP3 / HCLKP | HCLKP = positive sample clock | Test point |
| TP4 / HCLKN | HCLKN = negative sample clock | Test point |
| TP5 / VREFA | Between -1.8V and -2.2V | Test point |
| JU1 / VEED2 | | |
| JU2 / VCC2 | | |

Table 2: Component List

| DESIGNATOR | QTY | DESCRIPTION |
|------------------------|-----|-------------------------------------|
| C1-C19, C41, C42 | 21 | 22pF Capacitors (0603 size) |
| C20-C37, C40, C43, C44 | 21 | 0.1uF Capacitors (0603 size) |
| C38, C39, C45 | 3 | 0.1uF Capacitors (0805 size) |
| CP1 | 1 | 22uF Capacitor (3528 size) |
| CP2, CP3, CP4 | 3 | 4.7uF Capacitors (3528 size) |
| R1-R48 | 48 | 50Ω Resistor (0402 size) |
| R49, R55 | 2 | 120KΩ Resistor (0805 size) |
| R50, R56 | 2 | 200KΩ Potentiometer (64YPOT) |
| R51, R52 | 2 | 10KΩ Resistor (0805 size) |
| R53, R54 | 2 | RESERVED (0805 size) |
| R57, R60 | 2 | 250Ω Resistor (0805 size) |
| R58 | 1 | 50Ω Potentiometer (64YPOT) |
| R59 | 1 | 1250Ω Resistor (0805 size) |
| TF2 | 1 | Balun (ADTL2-18) |
| J20 | 1 | Edge Connector (QSE-080-01-F-D-EM2) |
| J1, J2, J3 | 3 | SMA Connector (142-0701-851) |
| BN1, BN2, BN3, BN4 | 4 | Banana Plug Sockets |
| JP1 | 1 | 2 Pin Header |
| JU1, JU2 | 2 | 3 Pin Header |
| LM1 | 1 | Adjustable Regulator (LM337) |
| RA1, RA2 | 2 | Shunt Regulator (TLV431ASNT1) |
| H2 | 1 | MUXDAC (RDA012M4-HD) |

Board Configuration

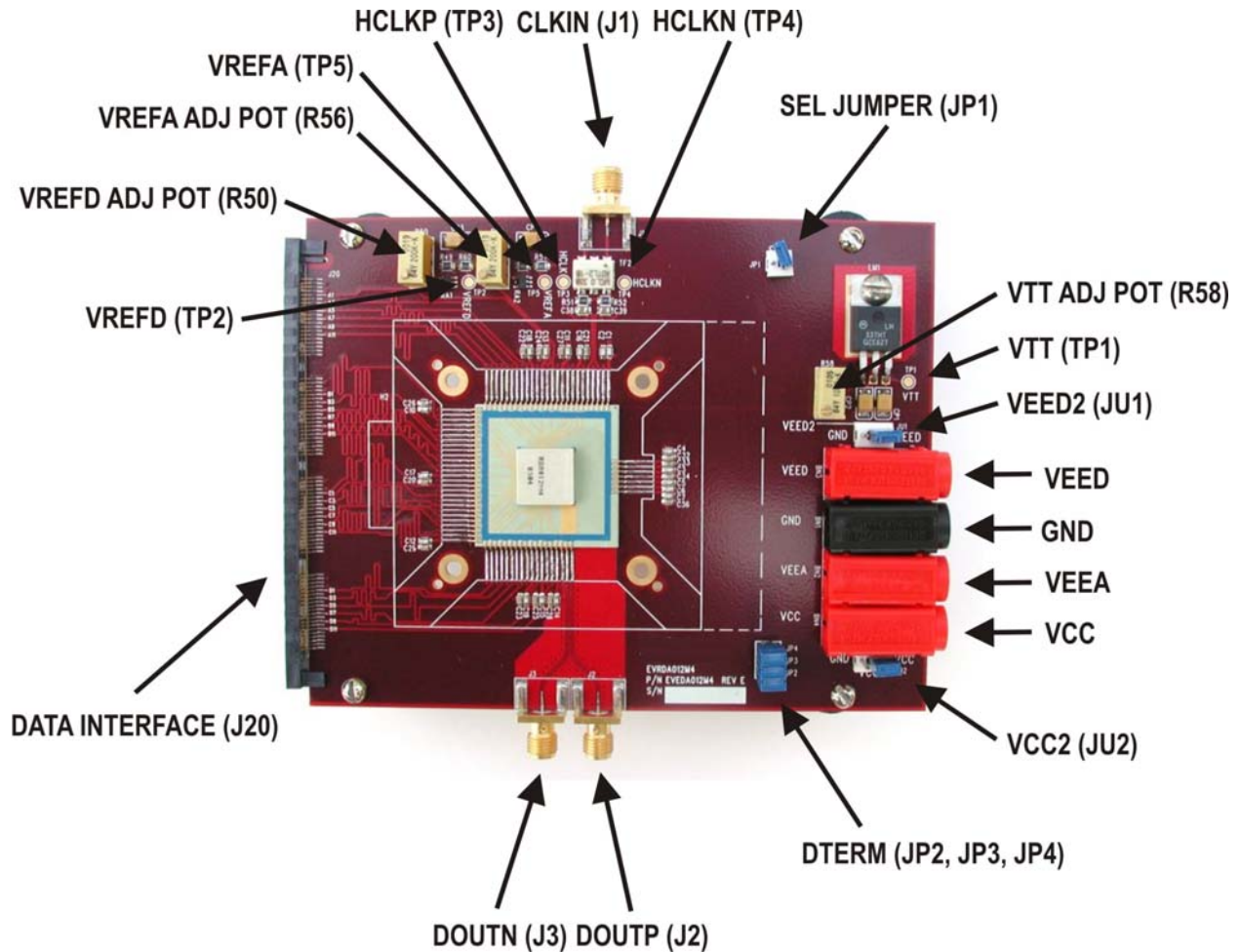


Figure 3 - EVRDA012M4 board configuration

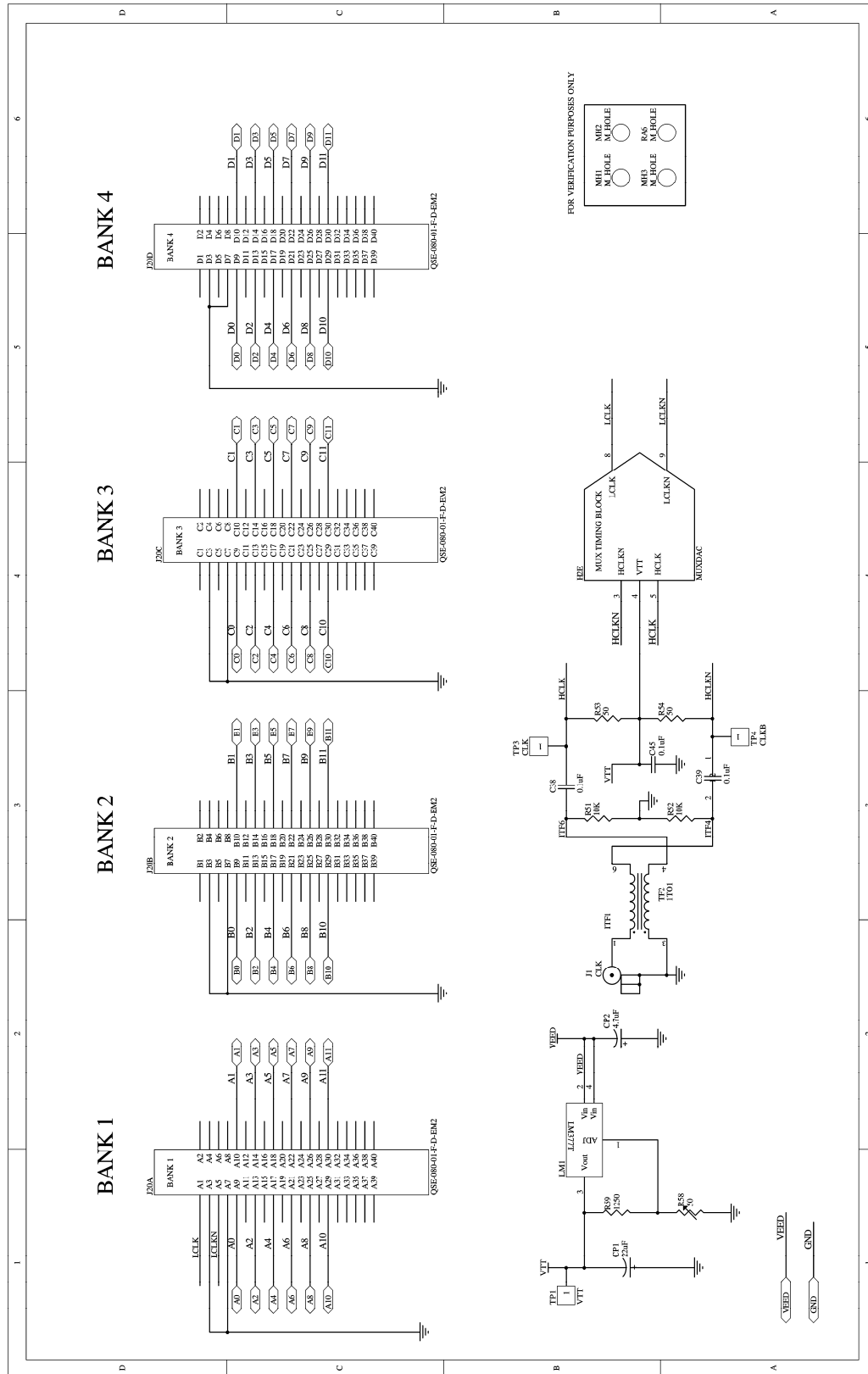


Figure 4 - EVRDA012M4 schematics (1)

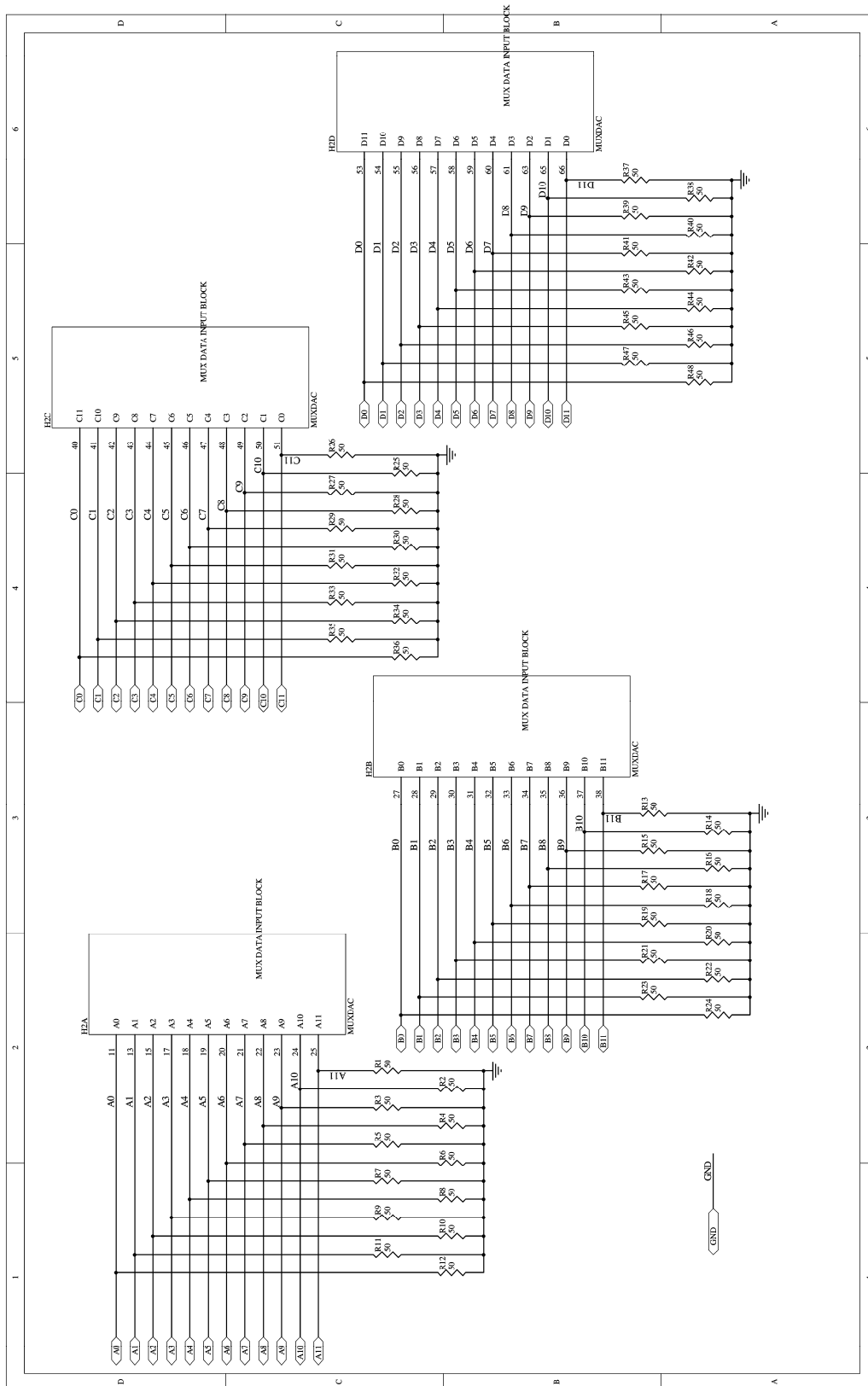


Figure 5 - EVRDA012M4 schematics (2)

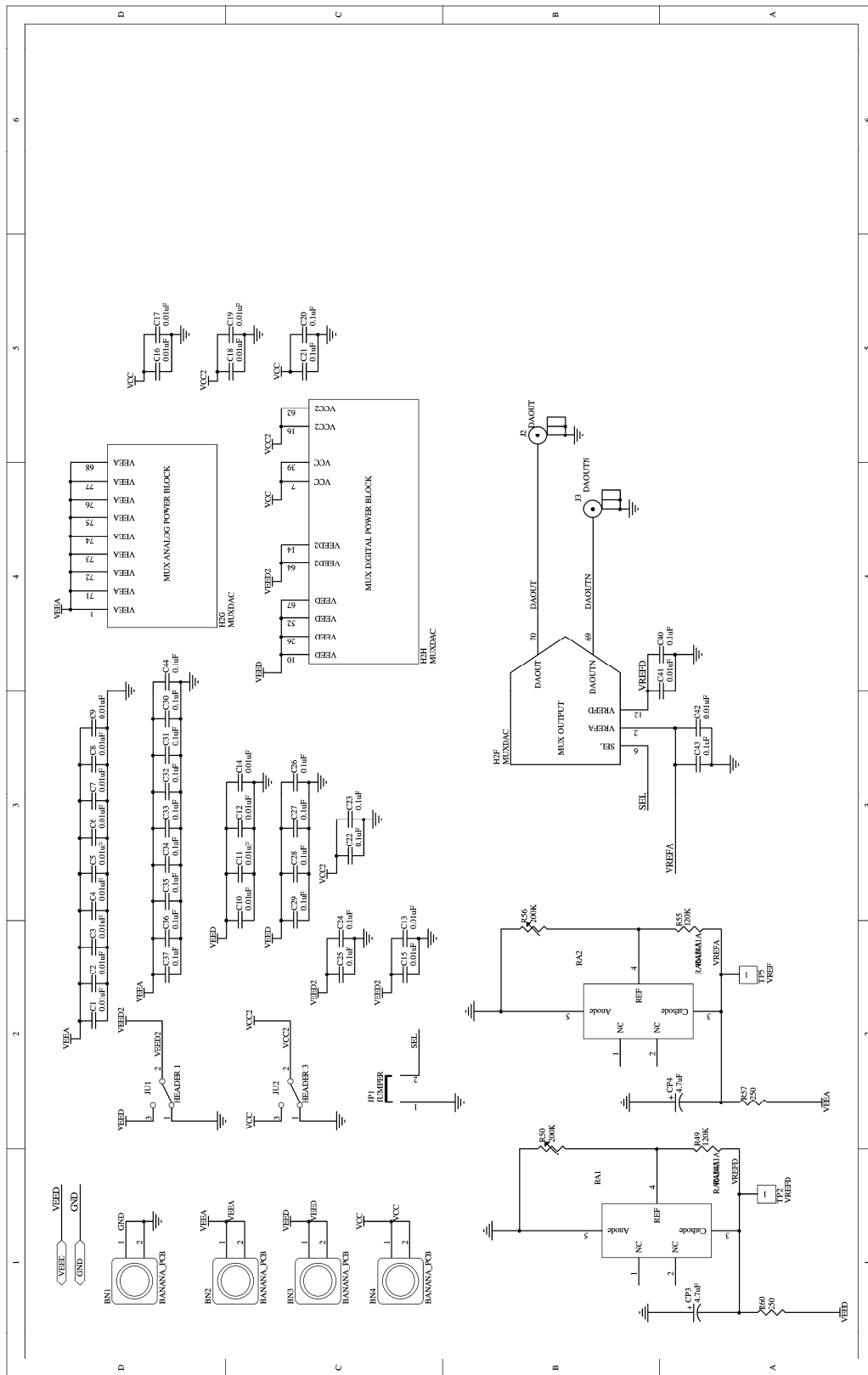


Figure 6 - EVRDA012M4 schematics (3)

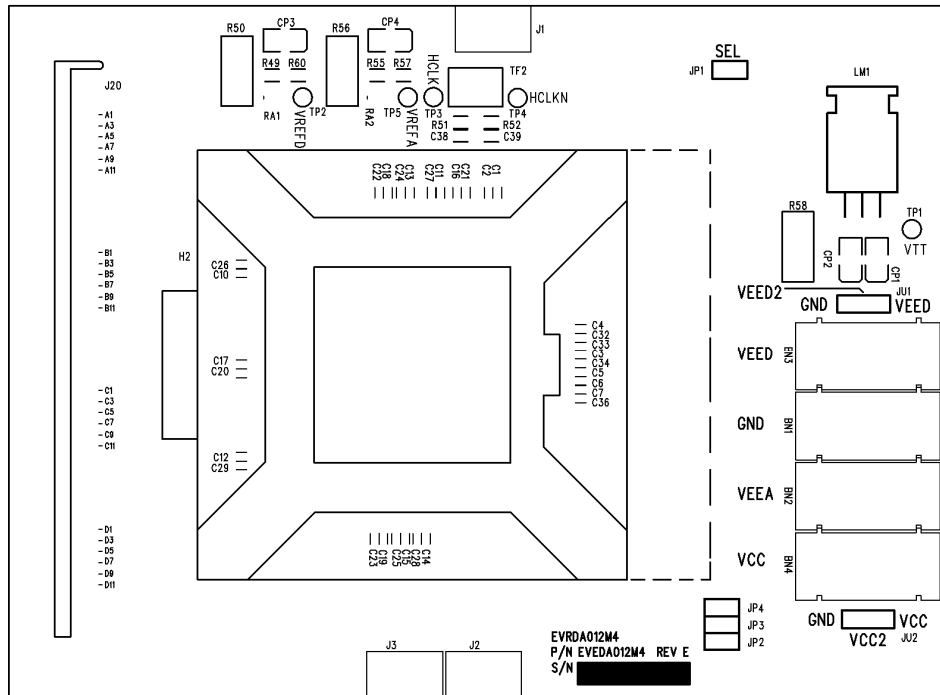


Figure 7 - Top layer stencil

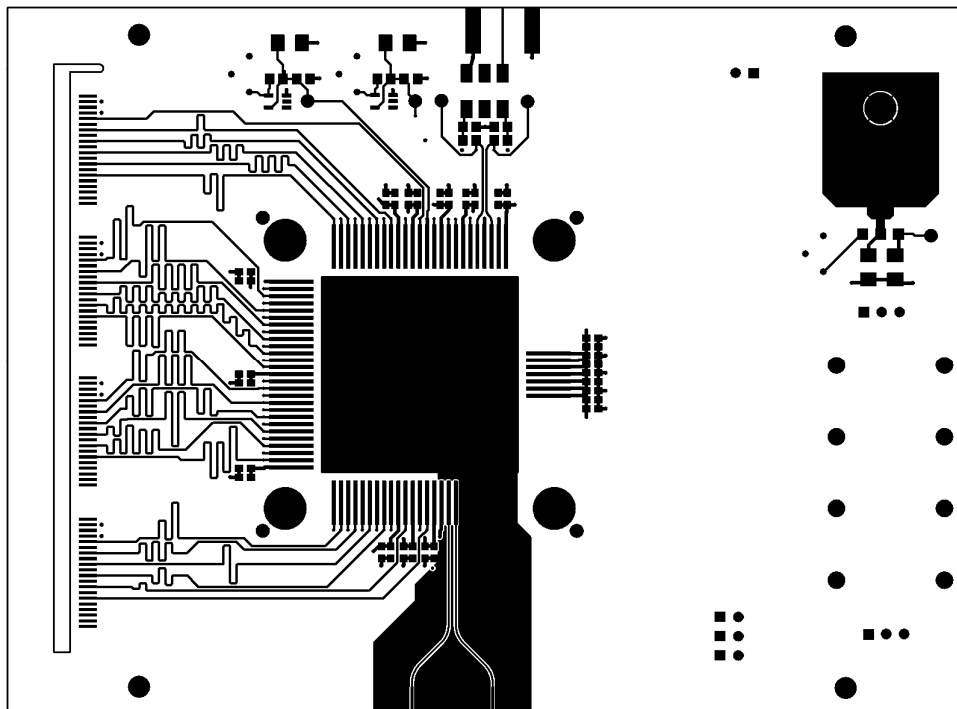


Figure 8 - Top layer

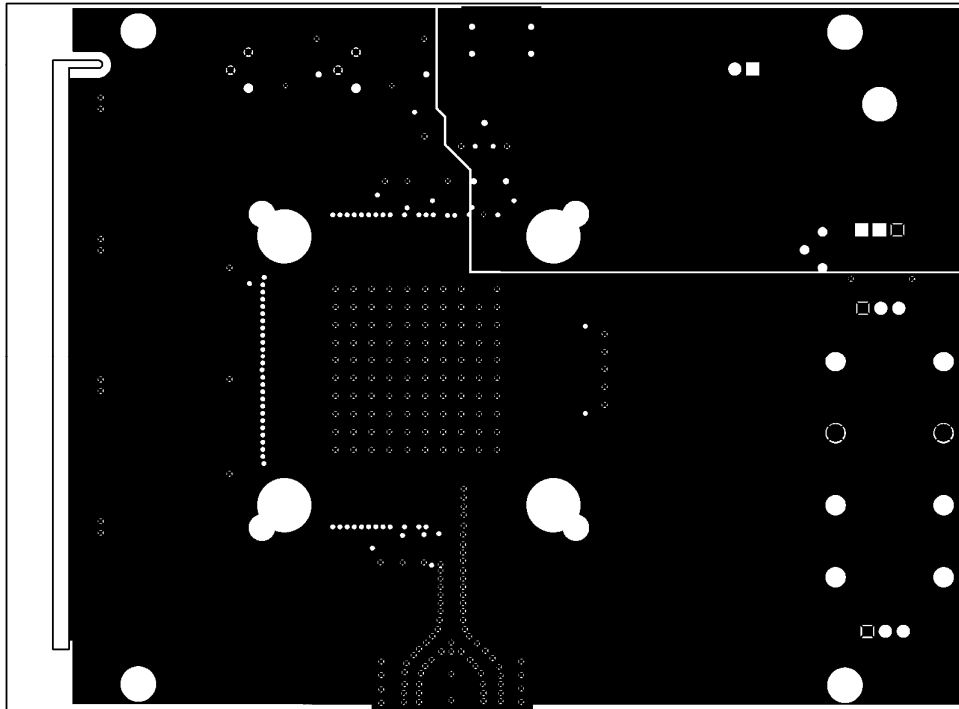


Figure 9 - GND and VTT

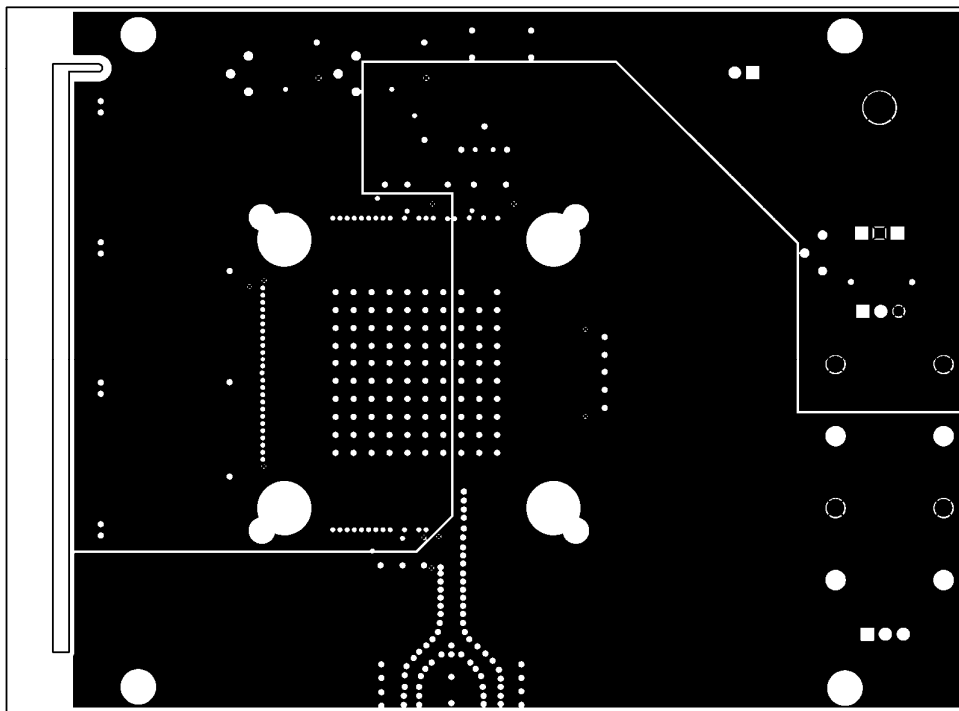


Figure 10 - VEEA and VEED

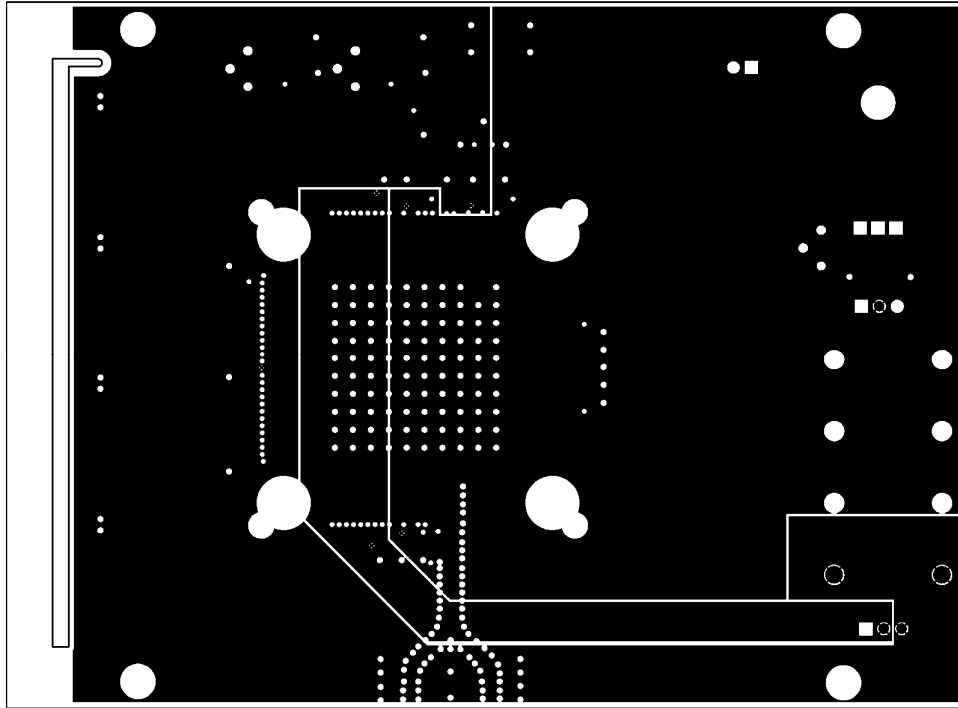


Figure 11 - VCC, VCC2 and VEED2

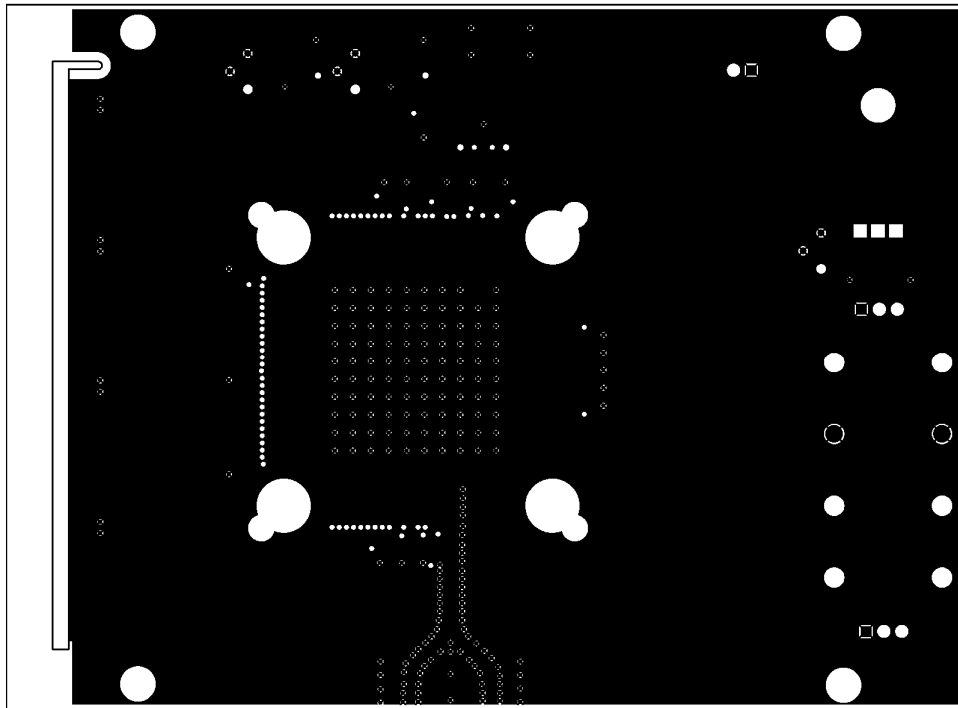


Figure 12 - GND

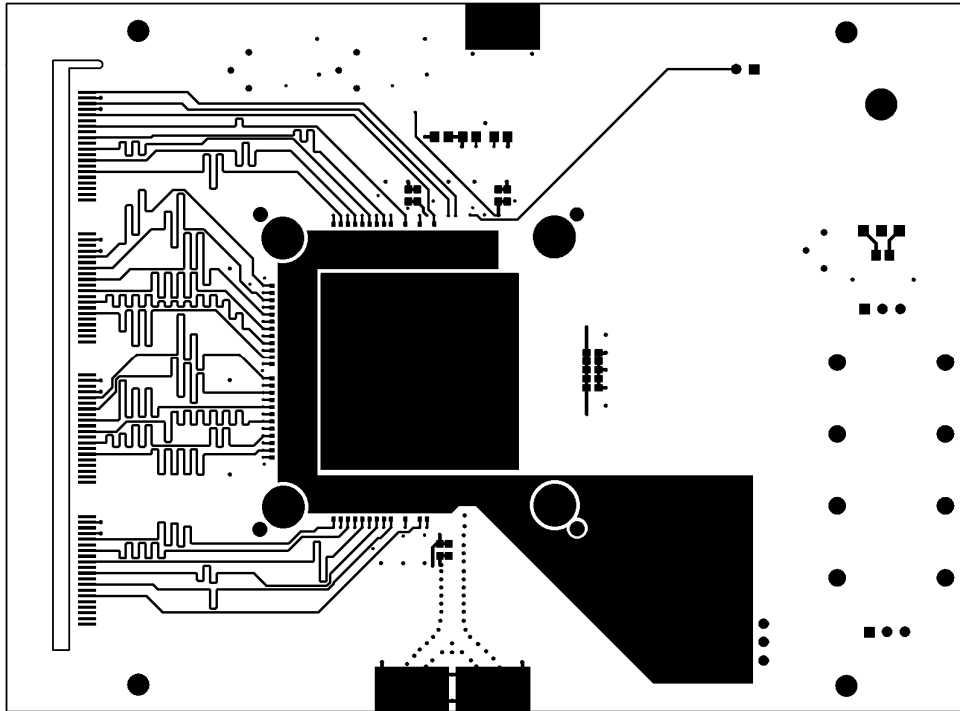


Figure 13 - Bottom layer

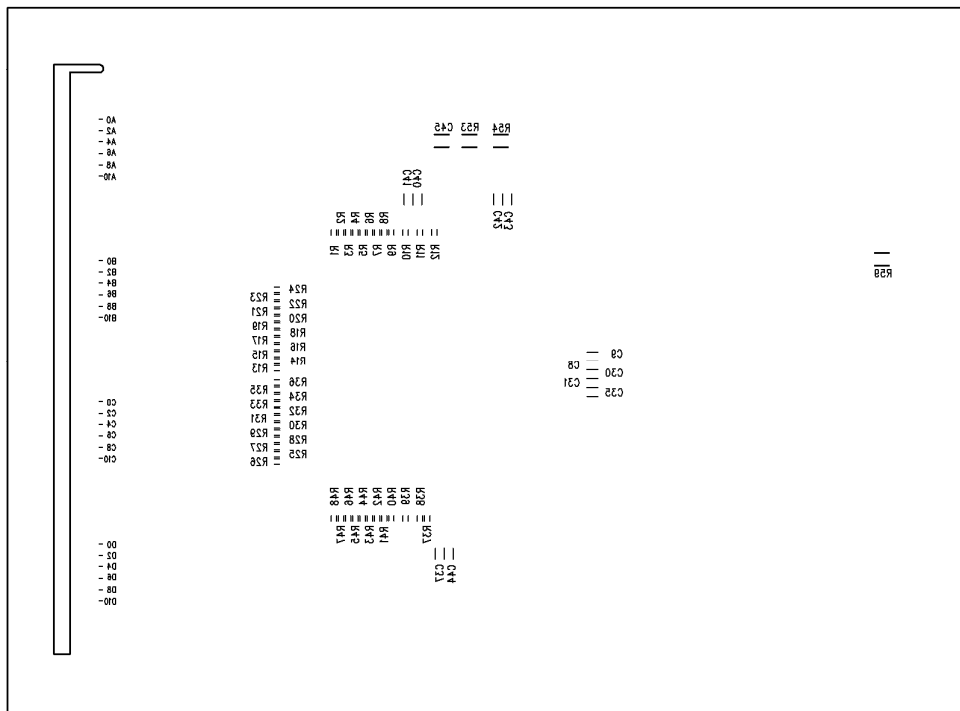


Figure 14 - Bottom layer stencil