TELEDYNE
SCIENTIFIC COMPANY

RTH090

25 GHz Bandwidth High Linearity Track-and-Hold

REV-DATE PA2-3215
FILE DS_0162PA2-3215

DS

RTH090

25 GHz Bandwidth High Linearity Track-and-Hold

Features

- 25 GHz Input Bandwidth
- Better than -40dBc THD Over the Total Bandwidth with Small Signal Input
- Better than 40dBc SFDR Over the Total Bandwidth with Small Signal Input
- 50 - 4000 MHz Sampling Rate
- Differential Analog Input/Output
- Output Held more than Half Clock Cycle
- 1.3W Power Dissipation
- Single Power Supply

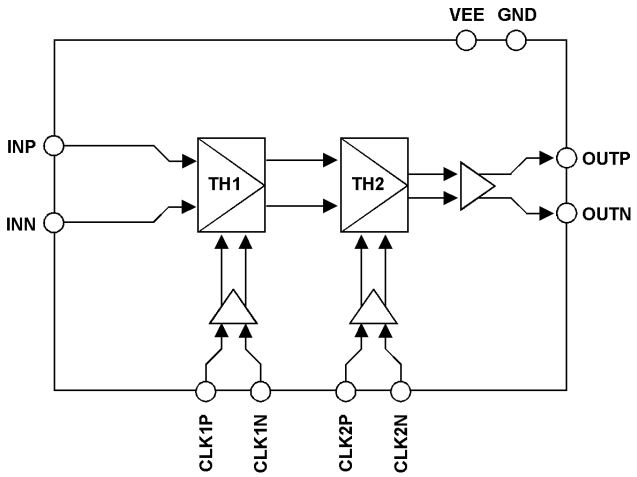

Figure 1 - Functional Block Diagram

Product Description

RTH090's bandwidth and aperture jitter enable 1 GS/s accurate sampling of DC to multi-GHz signals. The differential-to-differential dual track-and-hold cascades two track-and-hold circuits, TH1 and TH2. The RTH090 provides a held output for more than half a clock cycle, easing bandwidth requirements of subsequent circuitry relative to the case of a single track-and-hold (TH). The option to independently clock TH1 and TH2 further relaxes this requirement for sub-sampling applications.

Ordering information

PART NUMBER	DESCRIPTION
RTH090-HQ	24 Pin QFP Package
RTH090-DI	Die
EVRTH090	Evaluation Module

CAUTION
DEVICE SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD)

Absolute Maximum Ratings

Supply Voltages

VEE to GND ……..…….…..... -6 V

Input Voltages

INP, INN to GND ……..……..……-1 V
CLK1P, CLK1N, CLK2P, CLK2N to GND …….…… -1 V

Temperature

Case Temperature ……..…….....+125 °C
Junction Temperature ……..…….. +150 °C
Lead, Soldering (10 Seconds) …….. +220 °C
Storage …….. -40 to 125 °C

DC Electrical Specification

Test Conditions (see notes for specific conditions): Room Temperature; VEE = -5.0V; Clock: 1GHz, 0.8Vpp Differential; Input: 300mV Single-Ended; Differential Outputs Terminated Into 50 Ω to 0V.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
1.0	**DC TRANSFER FUNCTION**						
1.1	Gain	G			-6		dB
2.0	**TEMPERATURE DRIFT**						
2.1	Warm-up Time		After Power-up		1		s
3.0	**ANALOG INPUT (INP, INN)**						
3.1	Common Mode Voltage	IN_{CM}	Self Bias		-1.7		V
3.2	Input Resistance	R_{IN}	Each Lead to IN_{CM}		50		Ω
4.0	**CLOCK INPUTS (CLK1P, CLK1N, CLK2P, CLK2N)**						
4.1	Common Mode Voltage	CIN_{CM}	Self Bias		-2.4		V
4.2	Input Resistance	R_{CIN}	Each Lead to CIN_{CM}		50		Ω
5.0	**ANALOG OUTPUT (OUTP, OUTN)**						
5.1	Output Resistance	R_{OUT}	Each Output to GND		67		Ω
5.2	Maximum Current		Into Output Lead			10	mA
5.3	Common Mode Voltage	OUT_{CM}	No Input Signal 50Ohm Termination to GND		-280		mV
6.0	**POWER SUPPLY REQUIREMENTS**						
6.1	Negative Supply Current	IEE			250		mA
6.2	Power Dissipation	P			1.25		W

AC Electrical Specification – CLK = 1GHz

Test Conditions (see notes for specific conditions): Room Temperature; VEE = -5.0V; Clock: 1GHz, 0.8Vpp Differential; Differential Outputs Terminated Into 50 Ω to 0V.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
7.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.1Vpp SINGLE ENDED**						
7.1	Bandwidth	BW	-3dB Gain, 0.1 V_{PP} Single Ended Input		25		GHz
7.2	SFDR						
	60 MHz	SFDR	0.1 Vpp Single Ended Input		65		dBc
	2060 MHz	SFDR	0.1 Vpp Single Ended Input		62		dBc
	4060 MHz	SFDR	0.1 Vpp Single Ended Input		54		dBc
	6060 MHz	SFDR	0.1 Vpp Single Ended Input		50		dBc
	8060 MHz	SFDR	0.1 Vpp Single Ended Input		48		dBc
	10060 MHz	SFDR	0.1 Vpp Single Ended Input		46		dBc
	12060 MHz	SFDR	0.1 Vpp Single Ended Input		43		dBc
	14060 MHz	SFDR	0.1 Vpp Single Ended Input		40		dBc
	16060 MHz	SFDR	0.1 Vpp Single Ended Input		40		dBc
	18060 MHz	SFDR	0.1 Vpp Single Ended Input		47		dBc
	20060 MHz	SFDR	0.1 Vpp Single Ended Input		47		dBc
	22060 MHz	SFDR	0.1 Vpp Single Ended Input		42		dBc
	24060 MHz	SFDR	0.1 Vpp Single Ended Input		51		dBc
	26060 MHz	SFDR	0.1 Vpp Single Ended Input		50		dBc
	28060 MHz	SFDR	0.1 Vpp Single Ended Input		52		dBc
	30060 MHz	SFDR	0.1 Vpp Single Ended Input		44		dBc
7.3	THD						
	60 MHz	THD	0.1 Vpp Single Ended Input		-61		dBc
	2060 MHz	THD	0.1 Vpp Single Ended Input		-59		dBc
	4060 MHz	THD	0.1 Vpp Single Ended Input		-53		dBc
	6060 MHz	THD	0.1 Vpp Single Ended Input		-50		dBc
	8060 MHz	THD	0.1 Vpp Single Ended Input		-48		dBc
	10060 MHz	THD	0.1 Vpp Single Ended Input		-46		dBc
	12060 MHz	THD	0.1 Vpp Single Ended Input		-43		dBc
	14060 MHz	THD	0.1 Vpp Single Ended Input		-40		dBc
	16060 MHz	THD	0.1 Vpp Single Ended Input		-40		dBc
	18060 MHz	THD	0.1 Vpp Single Ended Input		-47		dBc
	20060 MHz	THD	0.1 Vpp Single Ended Input		-47		dBc
	22060 MHz	THD	0.1 Vpp Single Ended Input		-42		dBc
	24060 MHz	THD	0.1 Vpp Single Ended Input		-51		dBc
	26060 MHz	THD	0.1 Vpp Single Ended Input		-49		dBc
	28060 MHz	THD	0.1 Vpp Single Ended Input		-50		dBc
	30060 MHz	THD	0.1 Vpp Single Ended Input		-43		dBc

Test Conditions (see notes for specific conditions): Room Temperature; VEE = -5.0V; Clock: 1GHz, 0.8Vpp Differential; Differential Outputs Terminated Into 50 Ω to 0V.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
8.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.2Vpp SINGLE ENDED**						
8.1	Bandwidth	BW	-3dB Gain, 0.2 V_{PP} Single Ended Input		25		GHz
8.2	SFDR						
	60 MHz	SFDR	0.2 Vpp Single Ended Input		60		dBc
	2060 MHz	SFDR	0.2 Vpp Single Ended Input		56		dBc
	4060 MHz	SFDR	0.2 Vpp Single Ended Input		48		dBc
	6060 MHz	SFDR	0.2 Vpp Single Ended Input		44		dBc
	8060 MHz	SFDR	0.2 Vpp Single Ended Input		42		dBc
	10060 MHz	SFDR	0.2 Vpp Single Ended Input		40		dBc
	12060 MHz	SFDR	0.2 Vpp Single Ended Input		37		dBc
	14060 MHz	SFDR	0.2 Vpp Single Ended Input		34		dBc
	16060 MHz	SFDR	0.2 Vpp Single Ended Input		34		dBc
	18060 MHz	SFDR	0.2 Vpp Single Ended Input		41		dBc
	20060 MHz	SFDR	0.2 Vpp Single Ended Input		42		dBc
	22060 MHz	SFDR	0.2 Vpp Single Ended Input		36		dBc
	24060 MHz	SFDR	0.2 Vpp Single Ended Input		46		dBc
	26060 MHz	SFDR	0.2 Vpp Single Ended Input		44		dBc
	28060 MHz	SFDR	0.2 Vpp Single Ended Input		47		dBc
	30060 MHz	SFDR	0.2 Vpp Single Ended Input		39		dBc
8.3	THD						
	60 MHz	THD	0.2 Vpp Single Ended Input		-59		dBc
	2060 MHz	THD	0.2 Vpp Single Ended Input		-56		dBc
	4060 MHz	THD	0.2 Vpp Single Ended Input		-47		dBc
	6060 MHz	THD	0.2 Vpp Single Ended Input		-44		dBc
	8060 MHz	THD	0.2 Vpp Single Ended Input		-42		dBc
	10060 MHz	THD	0.2 Vpp Single Ended Input		-40		dBc
	12060 MHz	THD	0.2 Vpp Single Ended Input		-37		dBc
	14060 MHz	THD	0.2 Vpp Single Ended Input		-34		dBc
	16060 MHz	THD	0.2 Vpp Single Ended Input		-35		dBc
	18060 MHz	THD	0.2 Vpp Single Ended Input		-41		dBc
	20060 MHz	THD	0.2 Vpp Single Ended Input		-42		dBc
	22060 MHz	THD	0.2 Vpp Single Ended Input		-36		dBc
	24060 MHz	THD	0.2 Vpp Single Ended Input		-45		dBc
	26060 MHz	THD	0.2 Vpp Single Ended Input		-44		dBc
	28060 MHz	THD	0.2 Vpp Single Ended Input		-46		dBc
	30060 MHz	THD	0.2 Vpp Single Ended Input		-38		dBc

Test Conditions (see notes for specific conditions): Room Temperature; VEE = -5.0V; Clock: 1GHz, 0.8Vpp Differential; Differential Outputs Terminated Into 50 Ω to 0V.

9.0	DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.3Vpp SINGLE ENDED						
9.1	Bandwidth	BW	-3dB Gain, 0.3 V_{PP} Single Ended Input		25		GHz
9.2	SFDR						
	60 MHz	SFDR	0.3 Vpp Single Ended Input		57		dBc
	2060 MHz	SFDR	0.3 Vpp Single Ended Input		53		dBc
	4060 MHz	SFDR	0.3 Vpp Single Ended Input		44		dBc
	6060 MHz	SFDR	0.3 Vpp Single Ended Input		41		dBc
	8060 MHz	SFDR	0.3 Vpp Single Ended Input		38		dBc
	10060 MHz	SFDR	0.3 Vpp Single Ended Input		36		dBc
	12060 MHz	SFDR	0.3 Vpp Single Ended Input		34		dBc
	14060 MHz	SFDR	0.3 Vpp Single Ended Input		31		dBc
	16060 MHz	SFDR	0.3 Vpp Single Ended Input		31		dBc
	18060 MHz	SFDR	0.3 Vpp Single Ended Input		31		dBc
	20060 MHz	SFDR	0.3 Vpp Single Ended Input		38		dBc
	22060 MHz	SFDR	0.3 Vpp Single Ended Input		39		dBc
	24060 MHz	SFDR	0.3 Vpp Single Ended Input		42		dBc
	26060 MHz	SFDR	0.3 Vpp Single Ended Input		40		dBc
	28060 MHz	SFDR	0.3 Vpp Single Ended Input		43		dBc
	30060 MHz	SFDR	0.3 Vpp Single Ended Input		35		dBc
9.3	THD						
	60 MHz	THD	0.3 Vpp Single Ended Input		-57		dBc
	2060 MHz	THD	0.3 Vpp Single Ended Input		-54		dBc
	4060 MHz	THD	0.3 Vpp Single Ended Input		-50		dBc
	6060 MHz	THD	0.3 Vpp Single Ended Input		-43		dBc
	8060 MHz	THD	0.3 Vpp Single Ended Input		-41		dBc
	10060 MHz	THD	0.3 Vpp Single Ended Input		-39		dBc
	12060 MHz	THD	0.3 Vpp Single Ended Input		-36		dBc
	14060 MHz	THD	0.3 Vpp Single Ended Input		-33		dBc
	16060 MHz	THD	0.3 Vpp Single Ended Input		-35		dBc
	18060 MHz	THD	0.3 Vpp Single Ended Input		-48		dBc
	20060 MHz	THD	0.3 Vpp Single Ended Input		-42		dBc
	22060 MHz	THD	0.3 Vpp Single Ended Input		-34		dBc
	24060 MHz	THD	0.3 Vpp Single Ended Input		-50		dBc
	26060 MHz	THD	0.3 Vpp Single Ended Input		-47		dBc
	28060 MHz	THD	0.3 Vpp Single Ended Input		-54		dBc
	30060 MHz	THD	0.3 Vpp Single Ended Input		-47		dBc

AC Electrical Specification – CLK = 2GHz

Test Conditions (see notes for specific conditions): Room Temperature; VEE = -5.0V; Clock: 2GHz, 0.8Vpp Differential; Differential Outputs Terminated Into 50 Ω to 0V.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
10.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.1Vpp SINGLE ENDED**						
10.1	Bandwidth	BW	-3dB Gain, 0.1 V_{PP} Single Ended Input		25		GHz
10.2	SFDR						
	60 MHz	SFDR	0.1 Vpp Single Ended Input		66		dBc
	2060 MHz	SFDR	0.1 Vpp Single Ended Input		62		dBc
	4060 MHz	SFDR	0.1 Vpp Single Ended Input		54		dBc
	6060 MHz	SFDR	0.1 Vpp Single Ended Input		51		dBc
	8060 MHz	SFDR	0.1 Vpp Single Ended Input		48		dBc
	10060 MHz	SFDR	0.1 Vpp Single Ended Input		46		dBc
	12060 MHz	SFDR	0.1 Vpp Single Ended Input		44		dBc
	14060 MHz	SFDR	0.1 Vpp Single Ended Input		41		dBc
	16060 MHz	SFDR	0.1 Vpp Single Ended Input		41		dBc
	18060 MHz	SFDR	0.1 Vpp Single Ended Input		48		dBc
	20060 MHz	SFDR	0.1 Vpp Single Ended Input		48		dBc
	22060 MHz	SFDR	0.1 Vpp Single Ended Input		44		dBc
	24060 MHz	SFDR	0.1 Vpp Single Ended Input		53		dBc
	26060 MHz	SFDR	0.1 Vpp Single Ended Input		51		dBc
	28060 MHz	SFDR	0.1 Vpp Single Ended Input		53		dBc
	30060 MHz	SFDR	0.1 Vpp Single Ended Input		46		dBc
10.3	THD						
	60 MHz	THD	0.1 Vpp Single Ended Input		-61		dBc
	2060 MHz	THD	0.1 Vpp Single Ended Input		-59		dBc
	4060 MHz	THD	0.1 Vpp Single Ended Input		-54		dBc
	6060 MHz	THD	0.1 Vpp Single Ended Input		-50		dBc
	8060 MHz	THD	0.1 Vpp Single Ended Input		-48		dBc
	10060 MHz	THD	0.1 Vpp Single Ended Input		-46		dBc
	12060 MHz	THD	0.1 Vpp Single Ended Input		-44		dBc
	14060 MHz	THD	0.1 Vpp Single Ended Input		-41		dBc
	16060 MHz	THD	0.1 Vpp Single Ended Input		-41		dBc
	18060 MHz	THD	0.1 Vpp Single Ended Input		-48		dBc
	20060 MHz	THD	0.1 Vpp Single Ended Input		-48		dBc
	22060 MHz	THD	0.1 Vpp Single Ended Input		-44		dBc
	24060 MHz	THD	0.1 Vpp Single Ended Input		-52		dBc
	26060 MHz	THD	0.1 Vpp Single Ended Input		-50		dBc
	28060 MHz	THD	0.1 Vpp Single Ended Input		-51		dBc
	30060 MHz	THD	0.1 Vpp Single Ended Input		-44		dBc

Test Conditions (see notes for specific conditions): Room Temperature; VEE = -5.0V; Clock: 2GHz, 0.8Vpp Differential; Differential Outputs Terminated Into 50 Ω to 0V.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
11.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.2Vpp SINGLE ENDED**						
11.1	Bandwidth	BW	-3dB Gain, 0.2 V_{PP} Single Ended Input		25		GHz
11.2	SFDR						
	60 MHz	SFDR	0.2 Vpp Single Ended Input		60		dBc
	2060 MHz	SFDR	0.2 Vpp Single Ended Input		56		dBc
	4060 MHz	SFDR	0.2 Vpp Single Ended Input		48		dBc
	6060 MHz	SFDR	0.2 Vpp Single Ended Input		45		dBc
	8060 MHz	SFDR	0.2 Vpp Single Ended Input		42		dBc
	10060 MHz	SFDR	0.2 Vpp Single Ended Input		40		dBc
	12060 MHz	SFDR	0.2 Vpp Single Ended Input		38		dBc
	14060 MHz	SFDR	0.2 Vpp Single Ended Input		35		dBc
	16060 MHz	SFDR	0.2 Vpp Single Ended Input		36		dBc
	18060 MHz	SFDR	0.2 Vpp Single Ended Input		42		dBc
	20060 MHz	SFDR	0.2 Vpp Single Ended Input		42		dBc
	22060 MHz	SFDR	0.2 Vpp Single Ended Input		38		dBc
	24060 MHz	SFDR	0.2 Vpp Single Ended Input		47		dBc
	26060 MHz	SFDR	0.2 Vpp Single Ended Input		45		dBc
	28060 MHz	SFDR	0.2 Vpp Single Ended Input		48		dBc
	30060 MHz	SFDR	0.2 Vpp Single Ended Input		40		dBc
11.3	THD						
	60 MHz	THD	0.2 Vpp Single Ended Input		-59		dBc
	2060 MHz	THD	0.2 Vpp Single Ended Input		-56		dBc
	4060 MHz	THD	0.2 Vpp Single Ended Input		-48		dBc
	6060 MHz	THD	0.2 Vpp Single Ended Input		-45		dBc
	8060 MHz	THD	0.2 Vpp Single Ended Input		-42		dBc
	10060 MHz	THD	0.2 Vpp Single Ended Input		-40		dBc
	12060 MHz	THD	0.2 Vpp Single Ended Input		-38		dBc
	14060 MHz	THD	0.2 Vpp Single Ended Input		-35		dBc
	16060 MHz	THD	0.2 Vpp Single Ended Input		-36		dBc
	18060 MHz	THD	0.2 Vpp Single Ended Input		-42		dBc
	20060 MHz	THD	0.2 Vpp Single Ended Input		-42		dBc
	22060 MHz	THD	0.2 Vpp Single Ended Input		-38		dBc
	24060 MHz	THD	0.2 Vpp Single Ended Input		-47		dBc
	26060 MHz	THD	0.2 Vpp Single Ended Input		-45		dBc
	28060 MHz	THD	0.2 Vpp Single Ended Input		-47		dBc
	30060 MHz	THD	0.2 Vpp Single Ended Input		-40		dBc

Test Conditions (see notes for specific conditions): Room Temperature; VEE = -5.0V; Clock: 1GHz, 0.8Vpp Differential; Differential Outputs Terminated Into 50 Ω to 0V.

12.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.3Vpp SINGLE ENDED**						
12.1	Bandwidth	BW	-3dB Gain, 0.3 V_{PP} Single Ended Input		25		GHz
12.2	SFDR						
	60 MHz	SFDR	0.3 Vpp Single Ended Input		57		dBc
	2060 MHz	SFDR	0.3 Vpp Single Ended Input		53		dBc
	4060 MHz	SFDR	0.3 Vpp Single Ended Input		45		dBc
	6060 MHz	SFDR	0.3 Vpp Single Ended Input		41		dBc
	8060 MHz	SFDR	0.3 Vpp Single Ended Input		39		dBc
	10060 MHz	SFDR	0.3 Vpp Single Ended Input		36		dBc
	12060 MHz	SFDR	0.3 Vpp Single Ended Input		34		dBc
	14060 MHz	SFDR	0.3 Vpp Single Ended Input		32		dBc
	16060 MHz	SFDR	0.3 Vpp Single Ended Input		32		dBc
	18060 MHz	SFDR	0.3 Vpp Single Ended Input		39		dBc
	20060 MHz	SFDR	0.3 Vpp Single Ended Input		39		dBc
	22060 MHz	SFDR	0.3 Vpp Single Ended Input		34		dBc
	24060 MHz	SFDR	0.3 Vpp Single Ended Input		44		dBc
	26060 MHz	SFDR	0.3 Vpp Single Ended Input		42		dBc
	28060 MHz	SFDR	0.3 Vpp Single Ended Input		44		dBc
	30060 MHz	SFDR	0.3 Vpp Single Ended Input		37		dBc
12.3	THD						
	60 MHz	THD	0.3 Vpp Single Ended Input		-56		dBc
	2060 MHz	THD	0.3 Vpp Single Ended Input		-52		dBc
	4060 MHz	THD	0.3 Vpp Single Ended Input		-44		dBc
	6060 MHz	THD	0.3 Vpp Single Ended Input		-41		dBc
	8060 MHz	THD	0.3 Vpp Single Ended Input		-39		dBc
	10060 MHz	THD	0.3 Vpp Single Ended Input		-36		dBc
	12060 MHz	THD	0.3 Vpp Single Ended Input		-34		dBc
	14060 MHz	THD	0.3 Vpp Single Ended Input		-32		dBc
	16060 MHz	THD	0.3 Vpp Single Ended Input		-32		dBc
	18060 MHz	THD	0.3 Vpp Single Ended Input		-39		dBc
	20060 MHz	THD	0.3 Vpp Single Ended Input		-39		dBc
	22060 MHz	THD	0.3 Vpp Single Ended Input		-34		dBc
	24060 MHz	THD	0.3 Vpp Single Ended Input		-43		dBc
	26060 MHz	THD	0.3 Vpp Single Ended Input		-41		dBc
	28060 MHz	THD	0.3 Vpp Single Ended Input		-44		dBc
	30060 MHz	THD	0.3 Vpp Single Ended Input		-37		dBc

AC Electrical Specification – CLK = 4GHz

Test Conditions (see notes for specific conditions): Room Temperature; VEE = -5.0V; Clock: 4GHz, 0.8Vpp Differential; Differential Outputs Terminated Into 50 Ω to 0V.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
13.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.1Vpp SINGLE ENDED**						
13.1	Bandwidth	BW	-3dB Gain, 0.1 V_{PP} Single Ended Input		25		GHz
13.2	SFDR						
	60 MHz	SFDR	0.1 Vpp Single Ended Input		65		dBc
	4060 MHz	SFDR	0.1 Vpp Single Ended Input		54		dBc
	8060 MHz	SFDR	0.1 Vpp Single Ended Input		48		dBc
	12060 MHz	SFDR	0.1 Vpp Single Ended Input		44		dBc
	16060 MHz	SFDR	0.1 Vpp Single Ended Input		41		dBc
	20060 MHz	SFDR	0.1 Vpp Single Ended Input		48		dBc
	24060 MHz	SFDR	0.1 Vpp Single Ended Input		53		dBc
	28060 MHz	SFDR	0.1 Vpp Single Ended Input		53		dBc
13.3	THD						
	60 MHz	THD	0.1 Vpp Single Ended Input		-61		dBc
	4060 MHz	THD	0.1 Vpp Single Ended Input		-54		dBc
	8060 MHz	THD	0.1 Vpp Single Ended Input		-48		dBc
	12060 MHz	THD	0.1 Vpp Single Ended Input		-44		dBc
	16060 MHz	THD	0.1 Vpp Single Ended Input		-41		dBc
	20060 MHz	THD	0.1 Vpp Single Ended Input		-48		dBc
	24060 MHz	THD	0.1 Vpp Single Ended Input		-52		dBc
	28060 MHz	THD	0.1 Vpp Single Ended Input		-51		dBc
14.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.2Vpp SINGLE ENDED**						
14.1	Bandwidth	BW	-3dB Gain, 0.2 V_{PP} Single Ended Input		25		GHz
14.2	SFDR						
	60 MHz	SFDR	0.2 Vpp Single Ended Input		60		dBc
	4060 MHz	SFDR	0.2 Vpp Single Ended Input		48		dBc
	8060 MHz	SFDR	0.2 Vpp Single Ended Input		43		dBc
	12060 MHz	SFDR	0.2 Vpp Single Ended Input		38		dBc
	16060 MHz	SFDR	0.2 Vpp Single Ended Input		35		dBc
	20060 MHz	SFDR	0.2 Vpp Single Ended Input		43		dBc
	24060 MHz	SFDR	0.2 Vpp Single Ended Input		47		dBc
	28060 MHz	SFDR	0.2 Vpp Single Ended Input		48		dBc
14.3	THD						
	60 MHz	THD	0.2 Vpp Single Ended Input		-59		dBc
	4060 MHz	THD	0.2 Vpp Single Ended Input		-48		dBc
	8060 MHz	THD	0.2 Vpp Single Ended Input		-42		dBc
	12060 MHz	THD	0.2 Vpp Single Ended Input		-38		dBc
	16060 MHz	THD	0.2 Vpp Single Ended Input		-35		dBc
	20060 MHz	THD	0.2 Vpp Single Ended Input		-42		dBc
	24060 MHz	THD	0.2 Vpp Single Ended Input		-47		dBc
	28060 MHz	THD	0.2 Vpp Single Ended Input		-47		dBc

Test Conditions (see notes for specific conditions): Room Temperature; VEE = -5.0V; Clock: 4GHz, 0.8Vpp Differential; Differential Outputs Terminated Into 50 Ω to 0V.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
15.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.3Vpp SINGLE ENDED**						
15.1	Bandwidth	BW	-3dB Gain, 0.3 V_{PP} Single Ended Input		25		GHz
15.2	SFDR						
	60 MHz	SFDR	0.3 Vpp Single Ended Input		56		dBc
	4060 MHz	SFDR	0.3 Vpp Single Ended Input		44		dBc
	8060 MHz	SFDR	0.3 Vpp Single Ended Input		39		dBc
	12060 MHz	SFDR	0.3 Vpp Single Ended Input		34		dBc
	16060 MHz	SFDR	0.3 Vpp Single Ended Input		32		dBc
	20060 MHz	SFDR	0.3 Vpp Single Ended Input		39		dBc
	24060 MHz	SFDR	0.3 Vpp Single Ended Input		44		dBc
	28060 MHz	SFDR	0.3 Vpp Single Ended Input		45		dBc
15.3	THD						
	60 MHz	THD	0.3 Vpp Single Ended Input		-54		dBc
	4060 MHz	THD	0.3 Vpp Single Ended Input		-44		dBc
	8060 MHz	THD	0.3 Vpp Single Ended Input		-39		dBc
	12060 MHz	THD	0.3 Vpp Single Ended Input		-34		dBc
	16060 MHz	THD	0.3 Vpp Single Ended Input		-32		dBc
	20060 MHz	THD	0.3 Vpp Single Ended Input		-39		dBc
	24060 MHz	THD	0.3 Vpp Single Ended Input		-44		dBc
	28060 MHz	THD	0.3 Vpp Single Ended Input		-44		dBc

Operating Conditions

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
16.0	**CLOCK INPUTS (CLK1P, CLK1N, CLK2P, CLK2N)**						
16.1	Amplitude	V_{CPP}	Single Ended	300	450	600	mVpp
16.2	Common Mode Voltage	V_{CCM}			-2.4		V
16.3	CLK1 Frequency	F_{CLK1}		50		4000	MHz
16.4	CLK2 Frequency	F_{CLK2}		50		4000	MHz
17.0	**ANALOG INPUT (INP, INN)**						
17.1	Full Scale Range	FSR	Differential			1000	mVpp
17.2	Common Mode Voltage	V_{CM}	When DC Coupled		-1.7		V
18.0	**ANALOG OUTPUT (OUTP, OUTN)**						
18.1	Ext. Termination Voltage	V_{TERM}			0		V
18.2	Ext. Termination Resistor	R_{TERM}	Required From Outputs To Vterm		50		Ω
19.0	**POWER SUPPLY REQUIREMENTS**						
19.1	Negative Supply Voltage	VEE		-5.2	-5.0	-4.8	V
20.0	**OPERATING TEMPERATURE**[1]						
20.1	Case Temperature	Tc		-40		85	°C

[1] The part is designed to maintain high performance operation within a case temperature range of -40 ~ 85°C and we recommend not to exceed the Absolute Maximum Temperature shown on page 2. For the best performance, operation within the specified temperature range with proper heat dissipation is recommended. The metal pad where the part is soldered should be connected to the ground plane with thermal vias for better heat dissipation. A heatsink can be attached to the bottom of the PCB, on a metal pad connected to the metal pad where the part is soldered.

Pin Description and Pin Out (24 Lead QFP Package)

P/I/O	PIN	NUM.	NAME	FUNCTION
P	2, 4, 6, 10, 14, 16, 18, 22, bottom plate	8	GND	Power Supply Ground
P	1, 19, 21, 23	4	VEE	Negative Power Supply
I	9	1	CLK1P	Clock 1 Input: High = TH1 in Track Mode
I	8	1	CLK1N	Low = TH1 in Hold Mode
I	12	1	CLK2P	Clock 2 Input: High = TH2 in Track Mode
I	11	1	CLK2N	Low = TH2 in Hold Mode
I	3	1	INP	Analog Input
I	5	1	INN	
O	15	1	OUTP	Analog Output
O	17	1	OUTN	
R	7, 13, 20, 24	3	NC	Reserved

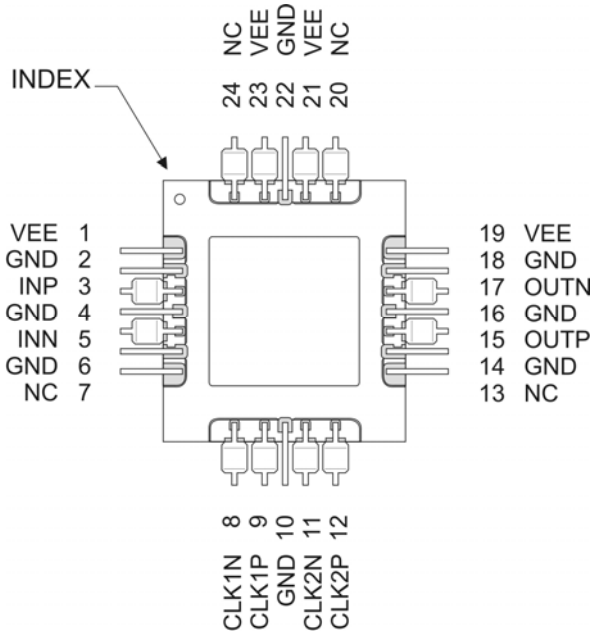

Figure 2 - RTH090 pinout (top view) 24 lead QFP package.

Definitions of Terms

Acquisition Time (tacq). The delay between the time a track-and-hold circuit (TH) enters track mode and the time the TH hold capacitor nodes track the input within some specified precision. The acquisition time sets a lower limit on the required track time during clocked operation.

Aperture Delay (ta). The average (or mean value) of the delay between the hold command (input clock switched from hold to track state) and the instant at which the analog input is sampled. The time is positive if the clock path delay is longer than the signal path delay. It is negative if the signal path delay is longer than the clock path delay.

Aperture Jitter (Δt). The standard deviation of the delay between the hold command (input clock switched from track-to-hold state) and the instant at which the analog input is sampled, excluding clock source jitter. It is the total jitter if the clock source is jitter free (ideal). Jitter diverges slowly as measurement time increases because of "1/f" noise, important at low frequencies (< 10 kHz). The specified jitter takes into account the white noise sources only (thermal and shot noise). For high-speed samplers this is reasonable, since even long data records span a time shorter than the time scale important for 1/f noise. For white-noise caused jitter, the clock and aperture jitter can be added in an rms manner to obtain the total sampling jitter.

Clock Jitter. The standard deviation of the mid-points of the relevant (rising or falling) edge of the clock source relative to the ideal edge (best fit). This jitter can be derived from the phase noise of the clock source, where the lower frequency bound of integration should correspond to the duration of a measurement record that the source will be used for.

Common-Mode Rejection Ratio (CMRR). Proportionality coefficient of the differential output and the common mode component of input signal. If an ideal symmetric input is available, CMR is the ratio of the differential output to the input on either input pin. A high-quality 50-ohm splitter may be used to generate the symmetrical inputs.

Full Scale Range (FSR). The maximum difference between the highest and lowest input levels for which various device performance specifications hold, unless otherwise noted.

Gain. Ratio of output signal magnitude to input signal magnitude. For sinewave inputs, it is the ratio of the amplitude of the first (main) harmonic output (HD1) to the amplitude of the input.

Input Bandwidth (BW). The input frequency at which the gain for sinewave input is reduced by 3 dB relative to its value at low frequencies. The low frequency range is defined as the range including DC over which the gain stays essentially constant. The high frequency range is characterized by an increase in gain variation versus frequency, at least including the eventual monotonic decrease of the gain ("roll-off"). The input bandwidth tends to be input amplitude dependent. It is normally largest for very small inputs and smallest for FSR inputs.

Settling Time (ts). The delay between the time that a track-and-hold circuit (TH) enters hold mode and the time that the TH hold capacitor nodes settle to within some specified precision. The settling time sets a lower limit on the required hold time during clocked operation.

Spurious Free Dynamic Range (SFDR). The ratio of the magnitude of the first (main) harmonic, HD1, and the highest other harmonic (or non-harmonic other tone, if present), as observed in the TH spectrum. The input is FSR, unless otherwise noted. SFDR in dB is given by 20log (SFDR as amplitude ratio), and is generally positive.

Total Harmonic Distortion (THD). The ratio of the square root of the sum of the harmonics 2 to 5 to the amplitude of the first (main) harmonic in the TH spectrum. THD in dB is given by 20log (THD as amplitude ratio), and is generally negative.

Theory of Operation

The RTH090 chip contains two TH's, TH1 and TH2, in series, together with clock shaping circuitry, BUFFER1 and BUFFER2, and a 50-ohm output driver, OUTBUF (Figure 1). To maximize dynamic range and insensitivity to noise, all non-DC internal circuits and all non-DC inputs and outputs are differential. TH1 determines the dynamic sampled-mode performance of the DTH. TH1 clock inputs, CLK1P and CLK1N, should be driven by a low-jitter clock source. TH2 is similar to TH1, except that its bandwidth requirement is lower.

The DTH receives a differential analog input signal at inputs INP and INN, which is sampled on the TH1 hold capacitors upon a falling transition of its differential clock voltage V(CLK1P) – V(CLK1N), after an aperture delay, ta, see Figure 3. TH1's aperture delay is positive, nominally 50ps.

The sampling instant is affected by clock source jitter (off-chip) and aperture jitter (caused by on-chip noise).

The held and buffered output of TH1, VTH1, is sampled on the TH2 hold capacitors upon a falling transition of its differential clock voltage V(CLK2P) – V(CLK2N), after an aperture delay closely equal to that of TH1. This allows simple out-of-phase clocking of TH1 and TH2 by having opposite phases for CLK1 and CLK2. Aperture jitter of TH2 is irrelevant, since the slew rate of the TH2 input is equal to the TH1 differential droop rate. TH2 can be in track mode before TH1 switches to hold, but a minimum track time of TH2 after TH1 enters hold mode must be observed to ensure that TH2 has fully acquired the TH1 output.

For out-of-phase clocking, the delay from the hold instant of TH1 to the ideal sampling time of circuitry after TH2 is close to one full clock cycle, for example 1 ns at a 1 GHz sampling rate, which eases the bandwidth requirement of subsequent circuitry. This is true, even though a small glitch will be present at the transition from track to hold of TH2. The output is accurate during the latter part of the clock cycle.

Lower limits for the sampling rates of TH1 and TH2 are set by single-ended hold-mode droop rates, and lead to the specification of maximum hold times. For longer hold times, the RTH090 must be allowed sufficient recovery time during track phase (or a sequence of track phases), so it can return to normal operation mode. The bandwidth of subsequent circuitry can be minimal if TH2 is clocked at its lowest recommended frequency.

Signal Descriptions

The absolute maximum rated voltage at input termination resistors is -1 V. The RTH090 is designed for 1 Vpp differential input signals. If operated in single-ended mode, the complementary input is self biased and can be left unconnected. Distortion in the single-ended mode will be higher than in differential mode, and differential input should be used for optimal performance. The INP and INN inputs are equivalent, except for the polarity of their effect on OUTP and OUTN.

Use differential clock signals for optimal performance. Large CLK1 edge rate benefits aperture jitter performance, small CLK1 and CLK2 amplitudes minimizes distortion due to clock feed-through in the higher clock frequency range. The RTH090 can also operate using single ended clocks. Distortion for single-ended clocks can be several dB higher than for differential clocks, and differential clocks should be used for optimal performance.

Due to its highly differential design, the RTH090 requires relatively modest power supply decoupling. The smaller decoupling capacitors from VEE to GND should be placed as close to the package as possible. Larger low frequency power supply decoupling capacitors, VEE to GND, should be placed within 1 inch of the RTH090. Depending on the expected noise on the supplies more capacitors in parallel may need to be used. With low-impedance supplies that are very quiet (no digital circuitry), the RTH090 can also perform well with no external decoupling at all.

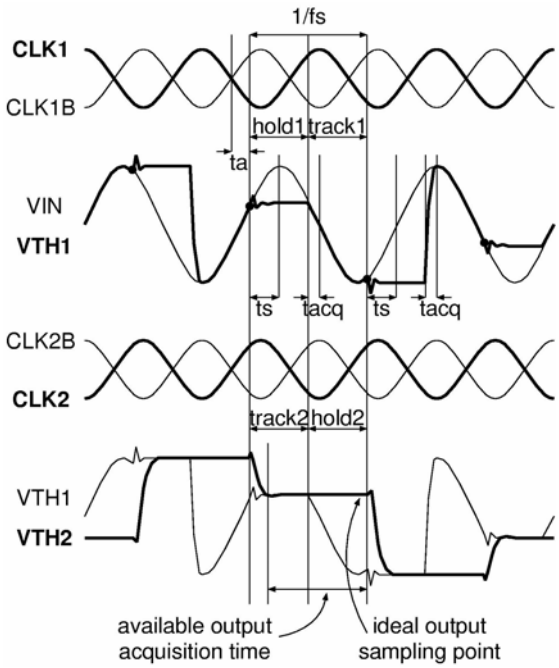

Figure 3 - Timing diagram for out-of-phase clocking of TH1 and TH2

Typical Operating Circuit

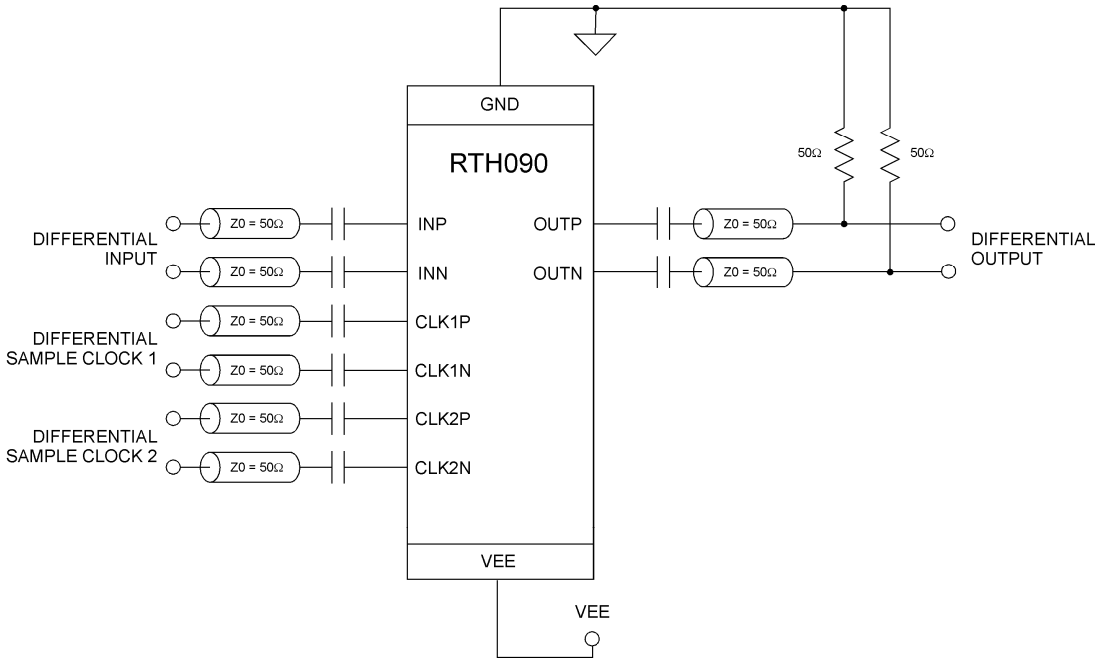

Figure 4 - Typical interface circuit. All differential IO are AC coupled.

Equivalent Circuit

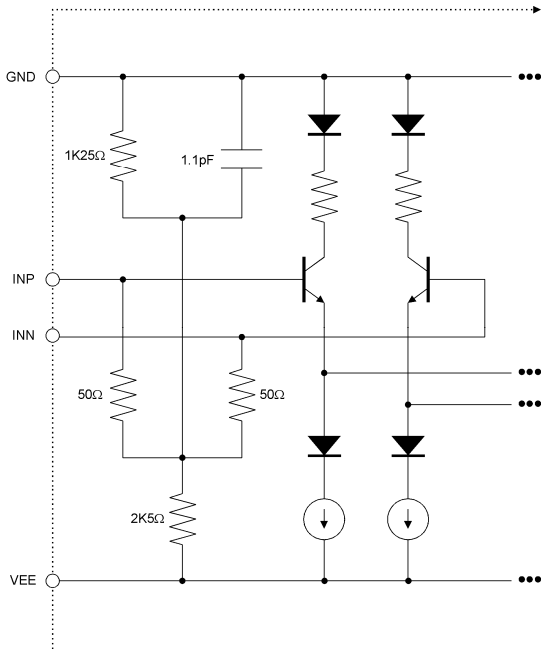

Figure 5 - Input circuit.

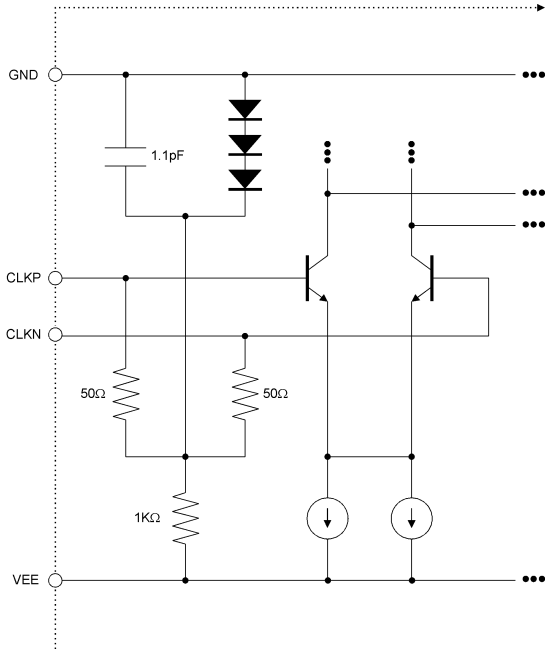

Figure 6- Clock circuit.

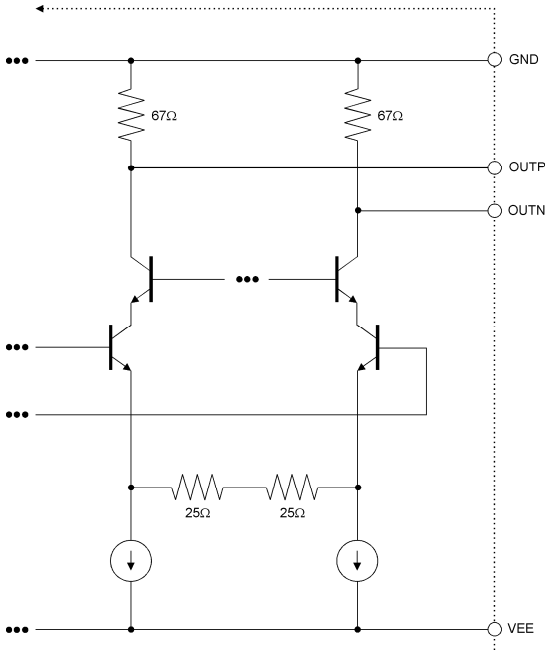

Figure 7- Output circuit.

Typical Performance (CLK = 1GHz)

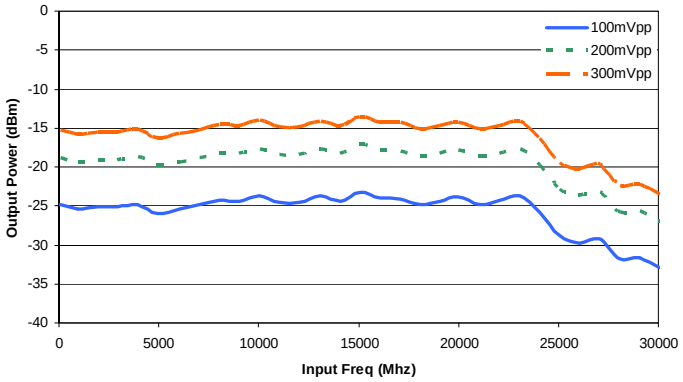

Figure 8- Input Bandwidth, single ended input.

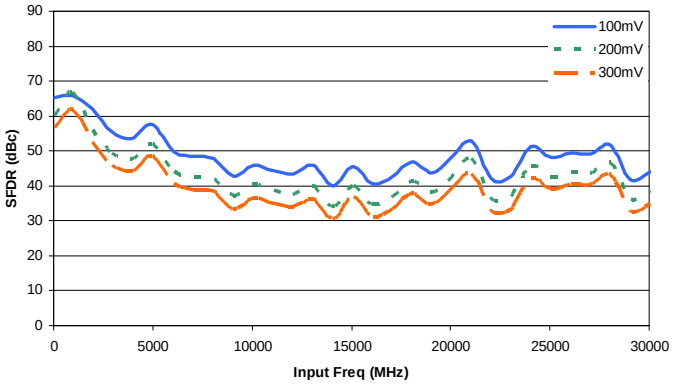

Figure 9- SFDR x Fin, single tone, single ended input.

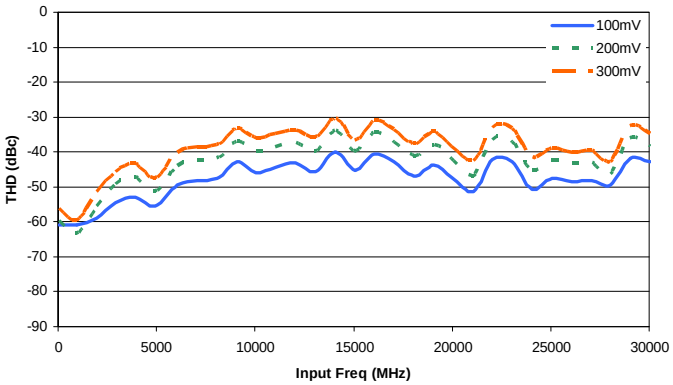

Figure 10- THD x Fin, single tone, single ended input.

Typical Performance (CLK = 2GHz)

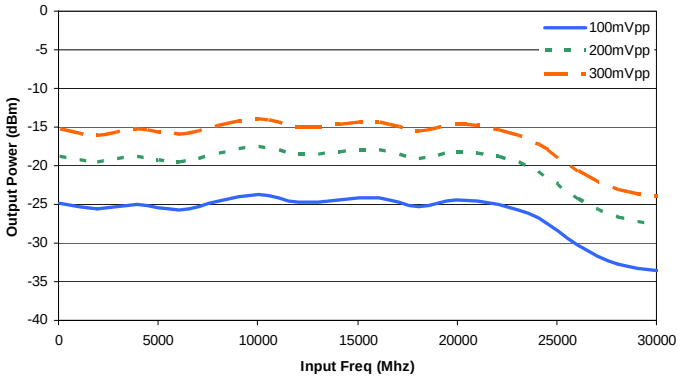

Figure 11 - Input Bandwidth, single ended input.

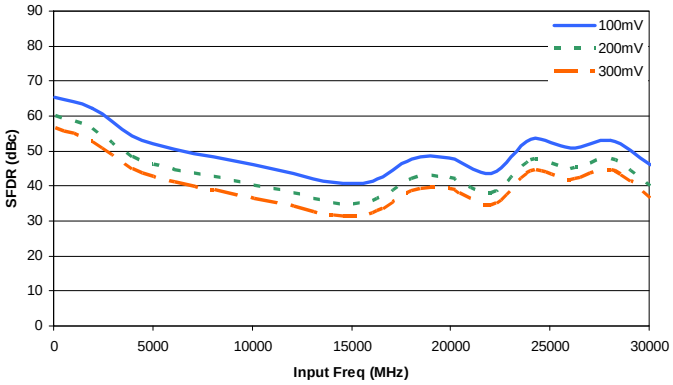

Figure 12 - SFDR x Fin, single tone, single ended input.

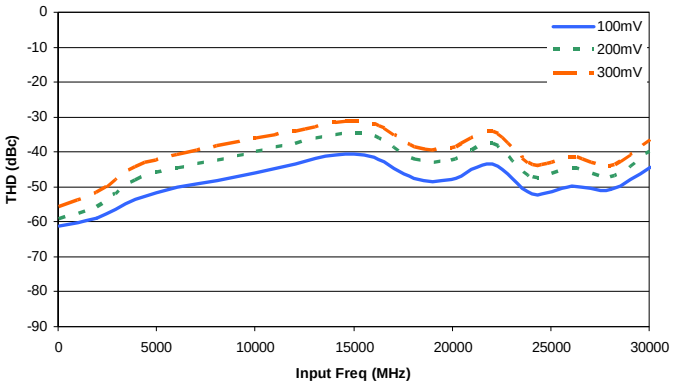

Figure 13 - THD x Fin, single tone, single ended input.

Typical Performance (CLK = 4GHz)

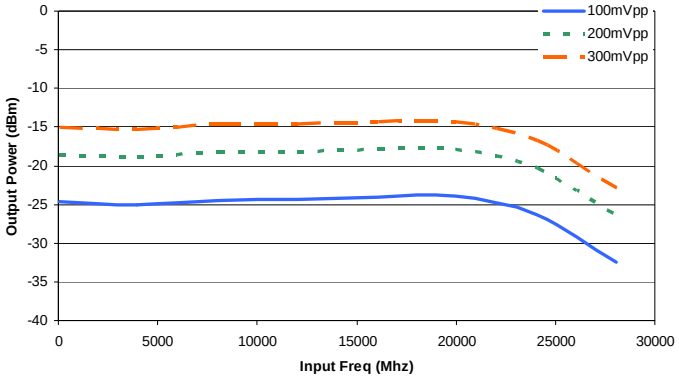

Figure 14 - Input Bandwidth, single ended input.

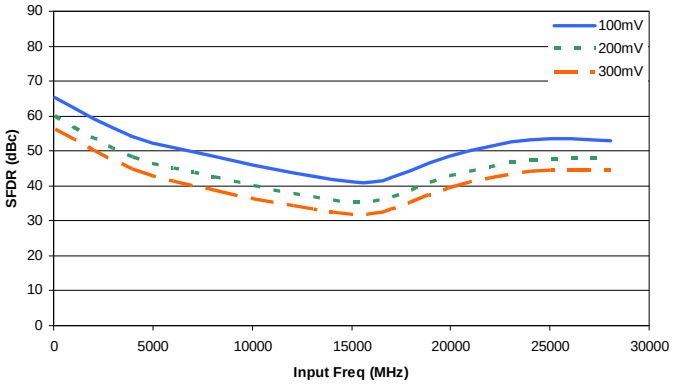

Figure 15 - SFDR x Fin, single tone, single ended input.

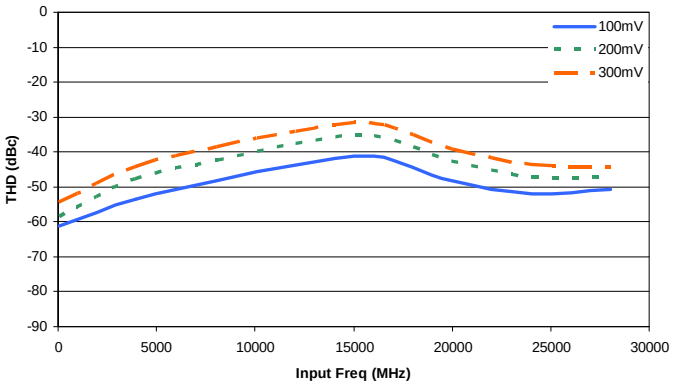

Figure 16 - THD x Fin, single tone, single ended input.

Package Information -HQ

The package is a high-speed 24 lead QFP with a Cu/Mo metal pad at the bottom.

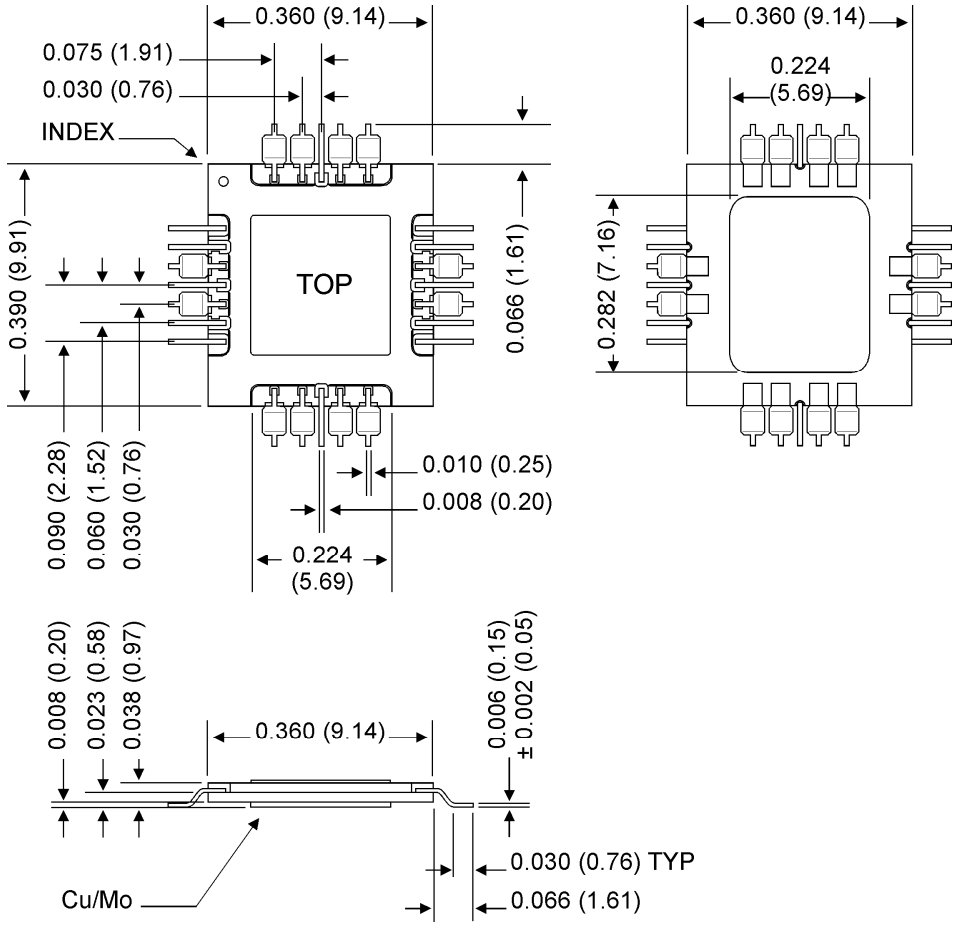

Figure 17 - RTH090-HQ package outline, dimensions in inches (mm).